

## **REMARKS**

Applicants will address each of the Examiner's objections and rejections in the order in which they appear in the Office Action.

### **Claim Objections**

In the Office Action, the Examiner objects to Claims 38 and 43 under 37 CFR §1.75(c) as being of improper dependent form. In particular, the Examiner states that Claims 38 and 43 are copies of corresponding preceding Claims 37 and 42, respectively.

In order to advance the prosecution of this application, Applicants have canceled Claims 38 and 42, rendering this objection moot. Accordingly, it is respectfully requested that this objection be withdrawn.

### **Claim Rejections - 35 USC §102**

The Examiner also rejects Claims 1-12 under 35 USC §102(e) as being anticipated by Kawasaki et al. This rejection is respectfully traversed.

More specifically, independent Claim 1 of the present application is directed to a light-emitting device, wherein all semiconductor elements constituting the pixel portion and the driver portion are n-channel type semiconductor elements.

In contrast, Kawasaki discloses CMOS including both N channel TFT and P channel TFT in Fig.7 (the office action cited col. 18, lns. 3-14 in Kawasaki which refer to Fig. 7 of the reference). Hence, Applicants believe that Kawasaki does not teach the claimed feature of "wherein all semiconductor elements constituting said pixel portion and said driver circuit are n-channel type

semiconductor elements" of independent Claim 1. For similar reasons, it is also believed that the reference does not disclose the features of independent Claim 7.

Accordingly, independent Claims 1 and 7 are not disclosed or suggested by the cited references but are patentable thereover. Therefore, it is respectfully requested that this rejection be withdrawn.

### Claim Rejections - 35 USC §103

#### Claims 13-18

The Examiner also rejects Claims 13-18 under 35 USC §103(a) as being unpatentable over Masuda et al. in view of Yamanaka et al. This rejection is also respectfully traversed.

More specifically, independent Claim 13 is directed to a light-emitting device wherein all semiconductor elements constituting the plurality of NAND circuits are n-channel type semiconductor elements. The Examiner admits that Masuda does not teach this feature. Accordingly, the Examiner cites Yamanaka as allegedly showing this feature.<sup>1</sup>

However, Yamanaka states that the "thin film transistors in the peripheral driving circuit region and the display region may be n-channel type, p-channel type or complementary type insulating gate electric field effect transistors; for example, the thin film transistors may comprise a combination of the complementary and n-channel types, a combination of the complementary and p-channel types, or a combination of the complementary, n-channel and p-channel types." (Col. 8, lns. 27-34). Hence, the reference fails to clearly teach the claimed feature of "wherein **all** semiconductor elements constituting said plurality of NAND circuit are n-channel type semiconductor elements." (emphasis added)

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<sup>1</sup> There is no showing in the Office Action as to where this feature is allegedly shown in Yamanaka.

Hence, Applicants respectfully submit that even if the combination of references was proper (which Applicants do not admit), one skilled in the art would not arrive at the claimed invention by combining these references. Accordingly, the rejected claims are patentable over the cited references, and it is respectfully requested that this rejection be withdrawn.

#### Claims 19-45

The Examiner also rejects Claims 19-45 under 35 USC §103(a) as being unpatentable over Masuda et al. in view of Yamanaka et al. in further view of Lei. This rejection is also respectfully traversed.

In the Office Action, the Examiner merely cites Lei for disclosing a gate of a transistor connected to a drain of a transistor. Therefore, since independent Claim 19 recites that all semiconductor elements constituting said buffer circuit are n-channel type semiconductor elements and independent Claim 24 recites that all semiconductor elements constituting said plurality of NAND circuits and said buffer circuit are n-channel thin film transistors, Claims 19-27 are patentable over the cited references for at least the reasons discussed above for Claims 13-18. Further, there has been no showing of where in the cited references the claimed feature of a buffer circuit is shown. Accordingly, it is respectfully requested that the rejection of these claims be withdrawn.

With respect to Claims 28-45, Lei discloses that for Fig. 7 (cited by the Examiner in support of the rejection), transistor 51 is an N channel depletion mode MOSFET (Col. 4, lns. 34-37 of Lei). Lei further discloses that for Fig. 9 (also cited by the Examiner in support of the rejection), an N channel enhancement mode MOSFET is substituted for the N channel depletion mode MOSFET of the transistor 51 of Fig. 7 (Col. 5, lns. 22-26 of Lei). Hence, transistor 51 in Lei is either an N

channel depletion mode MOSFET or an N channel enhancement mode MOSFET. Accordingly, Applicants respectfully submit that Lei fails to teach the claimed feature of "a plurality of flip-flop circuits formed by enhancement-type n-channel thin film transistors and depletion-type n-channel thin film transistors". As a result, even if the combination of these references is proper (which Applicants do not admit), one skilled in the art would not arrive at the light emitting device of Claim 28 by combining these references. Hence, Claim 28 is patentable over these references. For similar reasons, Applicants respectfully submit that Claims 29-45 are also patentable thereover. Accordingly, it is respectfully requested that this rejection be withdrawn.


#### Conclusion

It is respectfully submitted that the present application is in a condition for allowance, and it is requested that the application be allowed.

If any fee is due for this amendment, please charge our deposit account 50/1039.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,



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